CLAIMS

What is claimed is:

1. A decoder that is operable to perform hybrid decoding of an LDPC (Low Density Parity Check) coded modulation signal, the decoder comprising:

a symbol sequence estimate and symbol node update functional block that receives a plurality of symbol metrics corresponding to a symbol of a plurality of symbols of the LDPC coded modulation signal and also receives a plurality of initialized LLR (log likelihood ratio) bit edge messages;

wherein the plurality of bit edge messages corresponds to a plurality of edges that communicatively couple a plurality of symbol nodes to a plurality of check nodes within an LDPC coded modulation bipartite graph that corresponds to an LDPC code;

wherein the symbol sequence estimate and symbol node update functional block computes a first plurality of possible soft symbol estimates for the symbol;

wherein the symbol sequence estimate and symbol node update functional block updates a plurality of symbol node update bit edge messages using the received plurality of symbol metrics and the plurality of initialized LLR bit edge messages thereby generating a first updated plurality of symbol node update bit edge messages;

a check node update functional block that updates a plurality of check node update bit edge messages using the first updated plurality of symbol node update bit edge messages thereby generating a first updated plurality of check node update bit edge messages;

wherein the symbol sequence estimate and symbol node update functional block computes a second plurality of possible soft symbol estimates for the symbol using the first updated plurality of check node update bit edge messages;

wherein the symbol sequence estimate and symbol node update functional block updates the first updated plurality of symbol node update bit edge messages using the received plurality of symbol metrics and the first updated plurality of check node update bit edge messages thereby generating a second updated plurality of symbol node update bit edge messages;

wherein, during a last iterative decoding iteration, the symbol sequence estimate and symbol node update functional block makes a best estimate for the

symbol of the plurality of symbols of the LDPC coded modulation signal using that symbol's most recent corresponding plurality of possible soft symbol estimates; and

a hard limiter makes bit estimates based on the best estimate for the symbol such that the bit estimates are hard decisions for each of the individual bits of the symbol.

2. The decoder of claim 1, further comprising:

a syndrome calculator that determines whether each syndrome of a plurality of syndromes associated with the LDPC code is substantially equal to zero as defined by a predetermined degree of precision during each iterative decoding iteration; and

when, during a given iterative decoding iteration, the syndrome calculator determines that each of the syndromes of the plurality of syndromes associated with the LDPC code is substantially equal to zero as defined by the predetermined degree of precision, then the syndrome calculator determines that the given iterative decoding iteration is the last iterative decoding iteration.

3. The decoder of claim 1, wherein:

the updating of the plurality of symbol node update bit edge messages that is performed by the symbol sequence estimate and symbol node update functional block is mathematically performed in the logarithmic domain using min* processing.

4. The decoder of claim 1, wherein:

the updating of the plurality of check node update bit edge messages that is performed by the check node update functional block is mathematically performed in the logarithmic domain using min* processing.

5. The decoder of claim 1, wherein:

the symbol sequence estimate and symbol node update functional block estimates a partial binary vector selected from a plurality of partial binary vectors by summing over probabilities of a plurality of combined binary vectors;

the symbol sequence estimate and symbol node update functional block computes a plurality of label probabilities using the first updated plurality of check node update bit edge messages that is provided by the check node update functional block;

the symbol sequence estimate and symbol node update functional block computes extrinsic information of the selected partial binary vector;

the symbol sequence estimate and symbol node update functional block calculates a plurality of possible expanded binary vectors for a plurality of possible inserted bit values;

the symbol sequence estimate and symbol node update functional block computes extrinsic information of the plurality of possible expanded binary vectors for the plurality of possible inserted bit values; and

the symbol sequence estimate and symbol node update functional block updates the first updated plurality of symbol node update bit edge messages using the computed extrinsic information of the plurality of possible expanded binary vectors for the plurality of possible inserted bit values.

6. The decoder of claim 5, wherein:

each combined binary vectors of the plurality of combined binary vectors is generated using a partial binary vector and a remaining binary vector;

the partial binary vector is generated using a non-zero position vector; and

the remaining binary vector is generated using a zero position vector.

7. The decoder of claim 1, wherein:

the decoder performs hybrid decoding of a rate 2/3 8 PSK (8 Phase Shift Key) LDPC coded modulation signal having a block size of 14400; and

when the decoder operates at an E_b/N_o (ratio of energy per bit E_b to the Spectral Noise Density N_o) of approximately 3.5 dB (decibels), then the decoder supports a BER (Bit Error Rate) of approximately 1.25×10^{-8}.

8. The decoder of claim 1, wherein:

the LDPC coded modulation signal is a variable modulation signal;

a first symbol of the plurality of symbols is mapped according to a first modulation that includes a first constellation and a corresponding first mapping; and

a second symbol of the plurality of symbols is mapped according to a second modulation that includes a second constellation and a corresponding second mapping.

9. The decoder of claim 8, wherein:

the first modulation includes an 8 PSK (8 Phase Shift Key) shaped constellation whose constellation points are mapped according to the first mapping; and

the second modulation includes the 8 PSK shaped constellation whose constellation points are mapped according to the second mapping.

10. The decoder of claim 1, wherein:

the LDPC coded modulation signal is a variable code rate signal;

a first symbol of the plurality of symbols is encoded according to a first code rate; and

a second symbol of the plurality of symbols is encoded according to a second code rate.

11. The decoder of claim 1, wherein:

the decoder is implemented within a communication device; and

the communication device is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cellular communication system, a microwave communication system, a point-to-point communication system, a uni-directional communication system, a bi-directional communication system, a one to many communication system, a fiber-optic communication system, a WLAN (Wireless Local Area Network) communication system, and a DSL (Digital Subscriber Line) communication system.

12. A decoder that is operable to perform hybrid decoding of an LDPC (Low Density Parity Check) coded modulation signal, the decoder comprising:

a symbol sequence estimate and symbol node update functional block;

a check node update functional block that is communicatively coupled to the symbol sequence estimate and symbol node update functional block;

wherein the symbol sequence estimate and symbol node update functional block and the check node update functional block cooperatively perform iterative decoding processing of a symbol of a plurality of symbols of the LDPC coded modulation signal by successively and alternatively updating a plurality of bit edge messages;

wherein the plurality of bit edge messages corresponds to a plurality of edges that communicatively couple a plurality of symbol nodes to a plurality of check nodes within an LDPC coded modulation bipartite graph that corresponds to an LDPC code;

wherein the symbol sequence estimate and symbol node update functional block performs updating of the plurality of bit edge messages using a plurality of symbol metrics and the plurality of bit edge messages most recently updated by the check node update functional block;

wherein the plurality of symbol metrics correspond to the symbol of the plurality of symbols of the LDPC coded modulation signal; and

wherein the check node update functional block performs updating of the plurality of bit edge messages using the plurality of bit edge messages most recently updated by the symbol sequence estimate and symbol node update functional block.

13. The decoder of claim 12, wherein:

the symbol sequence estimate and symbol node update functional block computes a plurality of possible soft symbol estimates for the symbol during each decoding iteration.

14. The decoder of claim 13, wherein:

during a last iterative decoding iteration, the symbol sequence estimate and symbol node update functional block makes a best estimate for the symbol using that symbol's most recent corresponding plurality of possible soft symbol estimates; and further comprising:

a hard limiter that makes bit estimates based on the best estimate for the symbol such that the bit estimates are hard decisions for each of the individual bits of the symbol.

15. The decoder of claim 14, further comprising:

a syndrome calculator that determines whether each syndrome of a plurality of syndromes associated with the LDPC code is substantially equal to zero as defined by a predetermined degree of precision during each iterative decoding iteration; and

when, during a given iterative decoding iteration, the syndrome calculator determines that each of the syndromes of the plurality of syndromes associated with the LDPC code is substantially equal to zero as defined by the predetermined degree of precision, then the syndrome calculator determines that the given iterative decoding iteration is the last iterative decoding iteration.

16. The decoder of claim 12, wherein:

during a first iterative decoding iteration, a symbol metric computer provides the plurality of symbol metrics to the symbol sequence estimate and symbol node update functional block; and

during the first iterative decoding iteration, an LLR (log likelihood ratio) bit edge message initialization functional block provides a plurality of initialized LLR bit edge messages to the symbol sequence estimate and symbol node update functional block.

17. The decoder of claim 12, wherein:

the updating of the plurality of bit edge messages that is performed by the symbol sequence estimate and symbol node update functional block is mathematically performed in the logarithmic domain using min* processing.

18. The decoder of claim 12, wherein:

the updating of the plurality of bit edge messages that is performed by the check node update functional block is mathematically performed in the logarithmic domain using min* processing.

19. The decoder of claim 12, wherein:

the decoder performs hybrid decoding of a rate 2/3 8 PSK (8 Phase Shift Key) LDPC coded modulation signal having a block size of 14400; and

when the decoder operates at an E_b/N_o (ratio of energy per bit E_b to the Spectral Noise Density N_o) of approximately 3.5 dB (decibels), then the decoder supports a BER (Bit Error Rate) of approximately $1.25x10^{-8}$.

20. The decoder of claim 12, wherein:

the LDPC coded modulation signal is a variable modulation signal;

a first symbol of the plurality of symbols is mapped according to a first modulation that includes a first constellation and a corresponding first mapping; and

a second symbol of the plurality of symbols is mapped according to a second modulation that includes a second constellation and a corresponding second mapping.

21. The decoder of claim 20, wherein:

the first modulation includes an 8 PSK (8 Phase Shift Key) shaped constellation whose constellation points are mapped according to the first mapping; and

the second modulation includes the 8 PSK shaped constellation whose constellation points are mapped according to the second mapping.

22. The decoder of claim 12, wherein:

the LDPC coded modulation signal is a variable code rate signal;

a first symbol of the plurality of symbols is encoded according to a first code rate; and

a second symbol of the plurality of symbols is encoded according to a second code rate.

23. The decoder of claim 12, wherein:

the decoder is implemented within a communication device; and

the communication device is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cellular communication system, a microwave communication system, a point-to-point communication system, a uni-directional communication system, a bi-directional communication system, a one to many communication system, a fiber-optic communication system, a WLAN (Wireless Local Area Network) communication system, and a DSL (Digital Subscriber Line) communication system.

24. A decoding method that performs hybrid decoding of an LDPC (Low Density Parity Check) coded modulation signal, the method comprising:

receiving I, Q (In-phase, Quadrature) values corresponding to a symbol of a plurality of symbols of the LDPC coded modulation signal;

computing a plurality of symbol metrics corresponding to the symbol;

initializing a plurality of initialized LLR (log likelihood ratio) bit edge messages during an initial decoding iteration;

performing iterative decoding processing that includes performing symbol node updating and performing check node updating to update a plurality of bit edge messages;

wherein the symbol node updating includes:

computing a plurality of possible soft symbol estimates for the symbol during each decoding iteration;

updating the plurality of bit edge messages using the plurality of symbol metrics corresponding to the symbol and the plurality of bit edge messages most recently updated during check node updating;

wherein the check node updating includes:

updating the plurality of bit edge messages using a plurality of bit edge messages most recently updated during check node updating;

during a last iterative decoding iteration, making a best estimate for the symbol using that symbol's most recent corresponding plurality of possible soft symbol estimates; and

making bit estimates based on the best estimate for the symbol such that the bit estimates are hard decisions for each of the individual bits of the symbol.

25. The method of claim 24, further comprising:

determining whether each syndrome of a plurality of syndromes associated with the LDPC code is substantially equal to zero as defined by a predetermined degree of precision during each iterative decoding iteration; and

when, during a given iterative decoding iteration, it is determined that each of the syndromes of the plurality of syndromes associated with the LDPC code is substantially equal to zero as defined by the predetermined degree of precision, determining that the given iterative decoding iteration is the last iterative decoding iteration.

26. The method of claim 24, wherein the updating of the plurality of bit edge messages that is performed by the symbol node updating further comprises:

estimating a partial binary vector selected from a plurality of partial binary vectors by summing over probabilities of a plurality of combined binary vectors;

computing a plurality of label probabilities using the most recently updated plurality of bit edge messages that is updated by the check node updating;

computing extrinsic information of the selected partial binary vector;

calculating a plurality of possible expanded binary vectors for a plurality of possible inserted bit values;

computing extrinsic information of the plurality of possible expanded binary vectors for the plurality of possible inserted bit values; and

updating the plurality of bit edge messages using the computed extrinsic information of the plurality of possible expanded binary vectors for the plurality of possible inserted bit values.

27. The method of claim 26, further comprising:

generating each combined binary vectors of the plurality of combined binary vectors using a partial binary vector and a remaining binary vector;

generating the partial binary vector using a non-zero position vector; and

generating the remaining binary vector using a zero position vector.

28. The method of claim 24, wherein:

the updating of the plurality of bit edge messages that is performed by the symbol node updating is mathematically performed in the logarithmic domain using min* processing.

29. The method of claim 24, wherein:

the updating of the plurality of bit edge messages that is performed by the check node updating is mathematically performed in the logarithmic domain using min* processing.

30. The method of claim 24, wherein:

the method performs hybrid decoding of a rate 2/3 8 PSK (8 Phase Shift Key) LDPC coded modulation signal having a block size of 14400; and

when the method operates at an E_b/N_o (ratio of energy per bit E_b to the Spectral Noise Density N_o) of approximately 3.5 dB (decibels), then the method supports a BER (Bit Error Rate) of approximately 1.25×10^{-8}.

31. The method of claim 24, wherein:

the LDPC coded modulation signal is a variable modulation signal;

a first symbol of the plurality of symbols is mapped according to a first modulation that includes a first constellation and a corresponding first mapping; and

a second symbol of the plurality of symbols is mapped according to a second modulation that includes a second constellation and a corresponding second mapping.

32. The method of claim 31, wherein:

the first modulation includes an 8 PSK (8 Phase Shift Key) shaped constellation whose constellation points are mapped according to the first mapping; and

the second modulation includes the 8 PSK shaped constellation whose constellation points are mapped according to the second mapping.

33. The method of claim 24, wherein:

the LDPC coded modulation signal is a variable code rate signal;

a first symbol of the plurality of symbols is encoded according to a first code rate; and

a second symbol of the plurality of symbols is encoded according to a second code rate.

34. The method of claim 24, wherein:

the method is performed within a decoder;

the decoder is implemented within a communication device; and

the communication device is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cellular communication system, a microwave communication system, a point-to-point communication system, a uni-directional communication system, a bi-directional communication system, a one to many communication system, a fiber-optic communication system, a WLAN (Wireless Local Area Network) communication system, and a DSL (Digital Subscriber Line) communication system.